

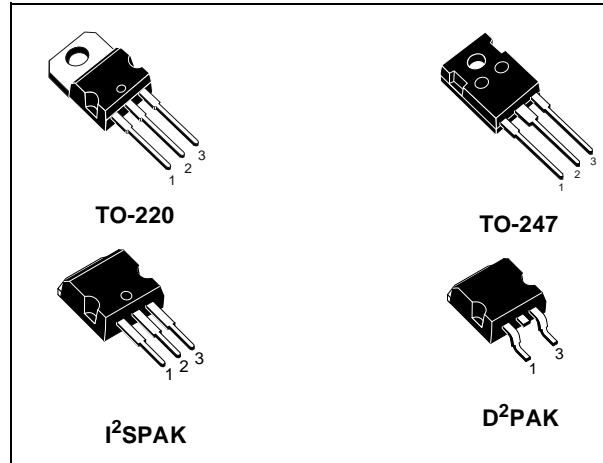


STP20NK50Z - STW20NK50Z STB20NK50Z - STB20NK50Z-S

N-CHANNEL 500V -0.23Ω- 17A TO-220/D²PAK/I²SPAK/TO-247
Zener-Protected SuperMESH™ MOSFET

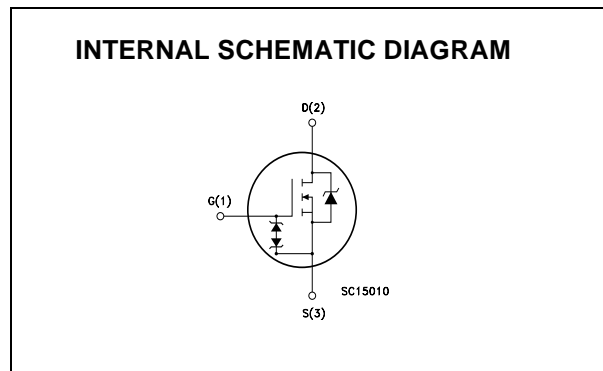
TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STB20NK50Z	500 V	< 0.27 Ω	17 A	190 W
STB20NK50Z-S	500 V	< 0.27 Ω	17 A	190 W
STP20NK50Z	500 V	< 0.27 Ω	17 A	190 W
STW20NK50Z	500 V	< 0.27 Ω	17 A	190 W

- TYPICAL R_{DS(on)} = 0.23 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY



DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB20NK50ZT4	B20NK50Z	D ² PAK	TAPE & REEL
STB20NK50Z-S	B20NK50Z	I ² SPAK	TUBE
STP20NK50Z	P20NK50Z	TO-220	TUBE
STW20NK50Z	W20NK50Z	TO-247	TUBE

STP20NK50Z - STB20NK50Z - STW20NK50Z - STB20NK50Z-S

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	500	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	500	V
V _{GS}	Gate- source Voltage	± 30	V
I _D	Drain Current (continuous) at T _C = 25°C	17	A
I _D	Drain Current (continuous) at T _C = 100°C	10.71	A
I _{DM} (•)	Drain Current (pulsed)	68	A
P _{TOT}	Total Dissipation at T _C = 25°C	190	W
	Derating Factor	1.51	W/°C
V _{ESD(G-S)}	Gate source ESD(HBM-C=100 pF, R=1.5 KΩ)	6000	V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	V/ns
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-55 to 150	°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 17A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220/D2PAK	TO-247	
R _{thj-case}	Thermal Resistance Junction-case Max	0.66		°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	62.5	50	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	17	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	850	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	I _{gs} = ± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

STP20NK50Z - STB20NK50Z - STW20NK50Z - STB20NK50Z-S

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0	500			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	3.75	4.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 8.5 A		0.23	0.27	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 15 V, I _D = 8.5 A		13		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		2600 328 72		pF pF pF
C _{oss eq.} (3)	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0V to 640V		187		pF

SWITCHING ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(on)} t _r t _{d(off)} t _f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V _{DD} = 250 V, I _D = 8.5 A R _G = 4.7Ω, V _{GS} = 10 V (Resistive Load see, Figure 3)		28 20 70 15		ns ns ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 400 V, I _D = 17 A, V _{GS} = 10 V		85 15.5 42	119	nC nC nC

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				17 68	A A
V _{SD} (1)	Forward On Voltage	I _{SD} = 17 A, V _{GS} = 0			1.6	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 17 A, di/dt = 100 A/μs V _R = 100 V, T _j = 25°C (see test circuit, Figure 5)		355 3.90 22		ns μC A
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 17 A, di/dt = 100 A/μs V _R = 100 V, T _j = 150°C (see test circuit, Figure 5)		440 5.72 26		ns μC A

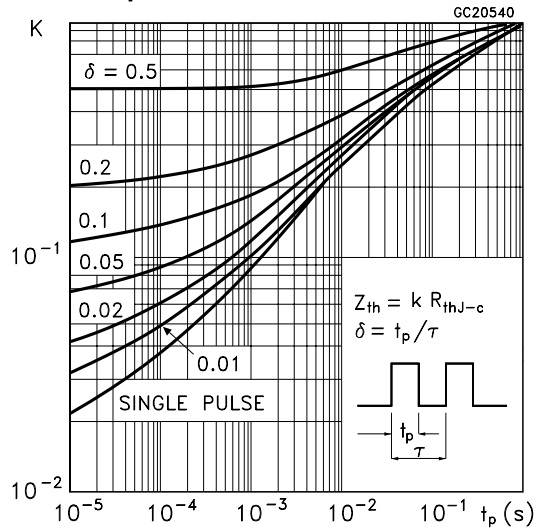
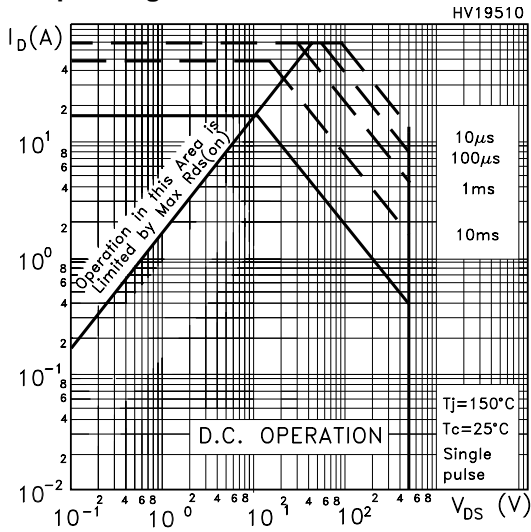
Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

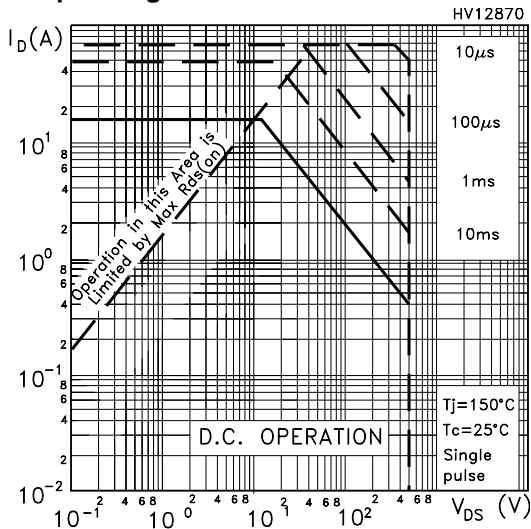
3. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

STP20NK50Z - STB20NK50Z - STW20NK50Z - STB20NK50Z-S

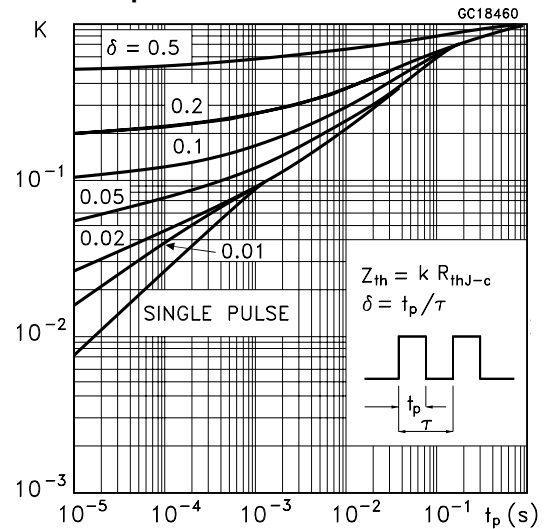
Safe Operating Area for TO-220 / D2PAK/ I2SPAK Thermal Impedance for TO-220 / D2PAK/I2SPAK



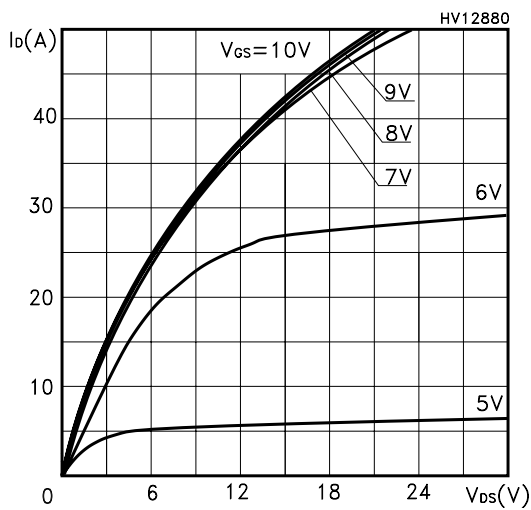
Safe Operating Area for TO-247



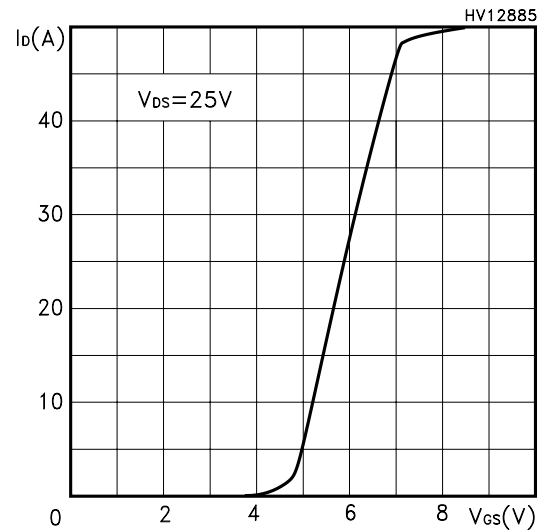
Thermal Impedance for TO-247



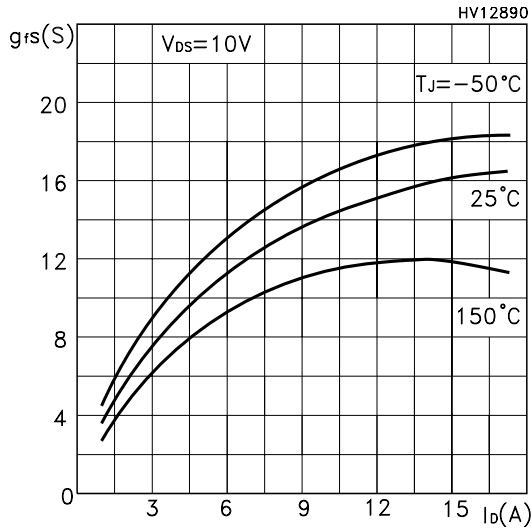
Output Characteristics



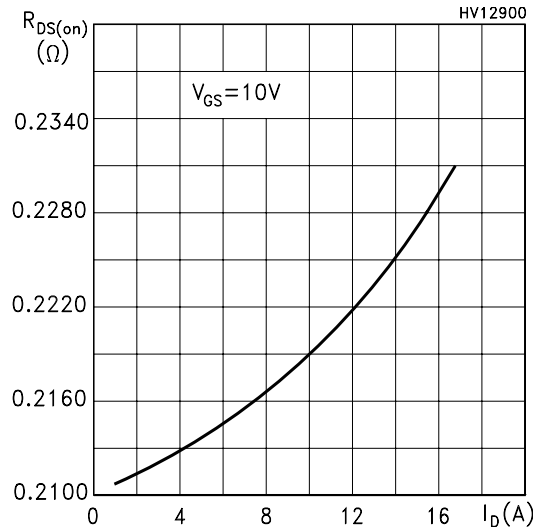
Transfer Characteristics



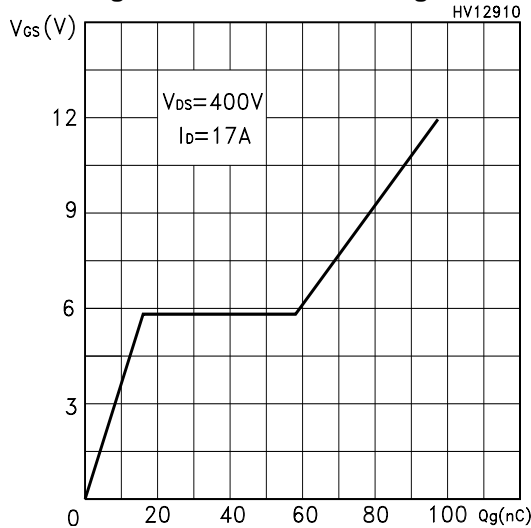
Transconductance



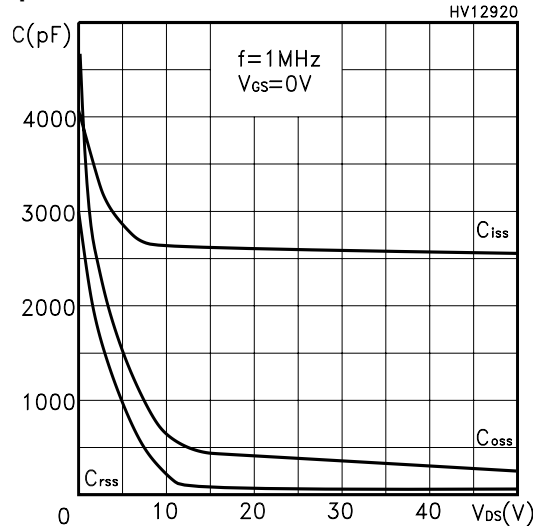
Static Drain-source On Resistance



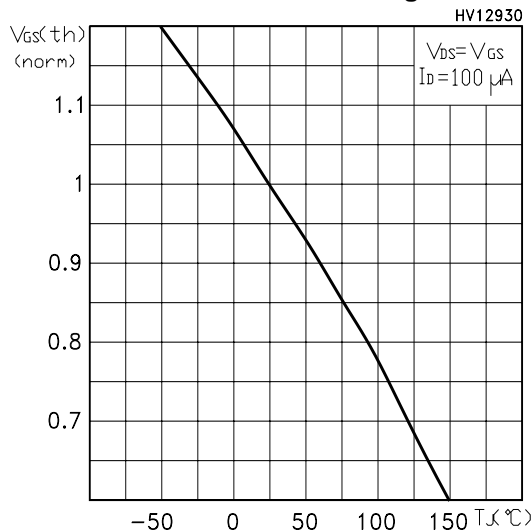
Gate Charge vs Gate-source Voltage



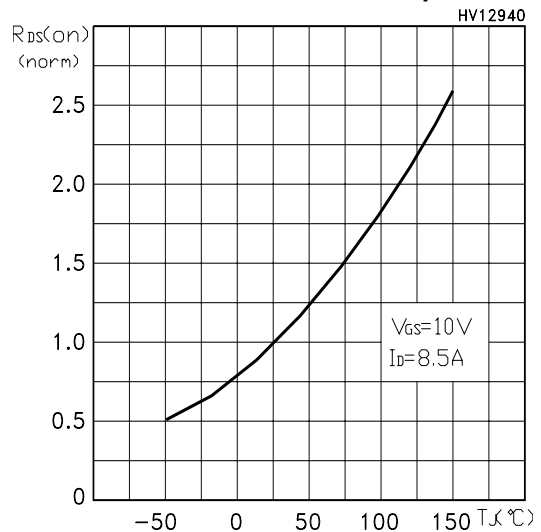
Capacitance Variations



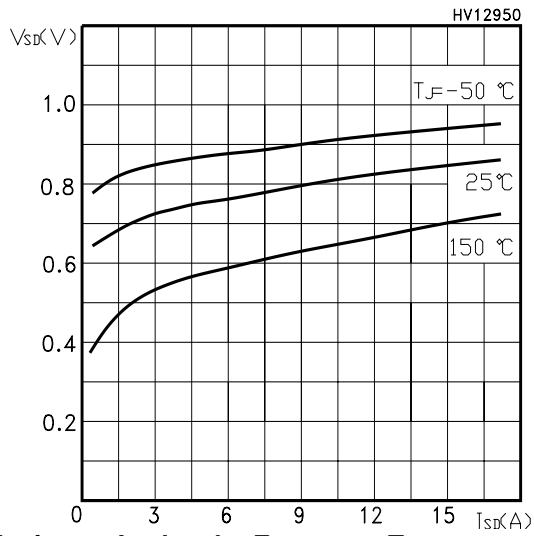
Normalized Gate Threshold Voltage vs Temp.



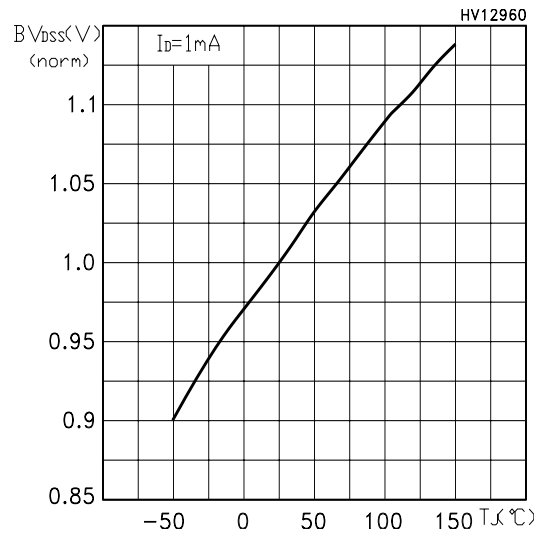
Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized BVDSS vs Temperature



Maximum Avalanche Energy vs Temperature

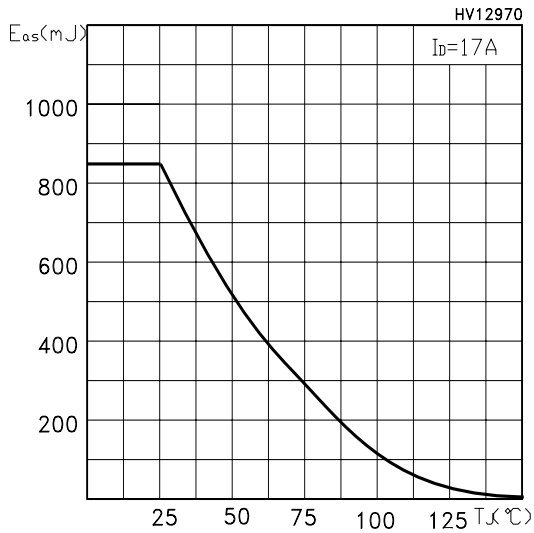


Fig. 1: Unclamped Inductive Load Test Circuit



Fig. 2: Unclamped Inductive Waveform



Fig. 3: Switching Times Test Circuit For Resistive Load



Fig. 4: Gate Charge test Circuit

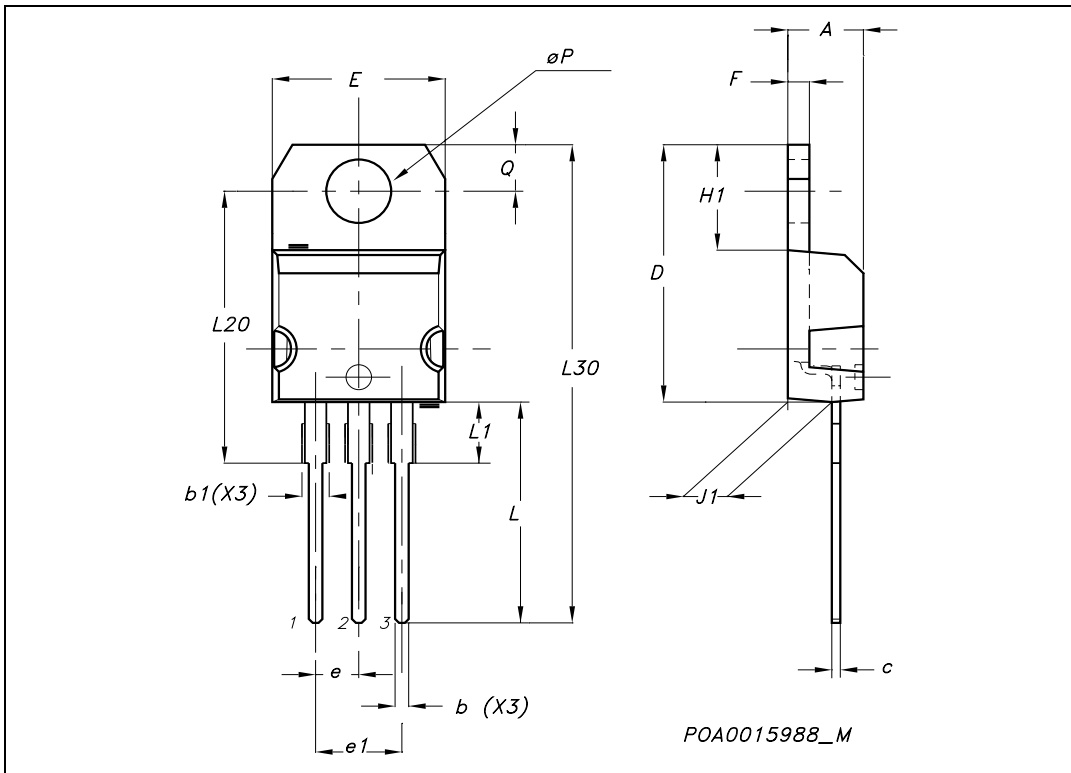


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



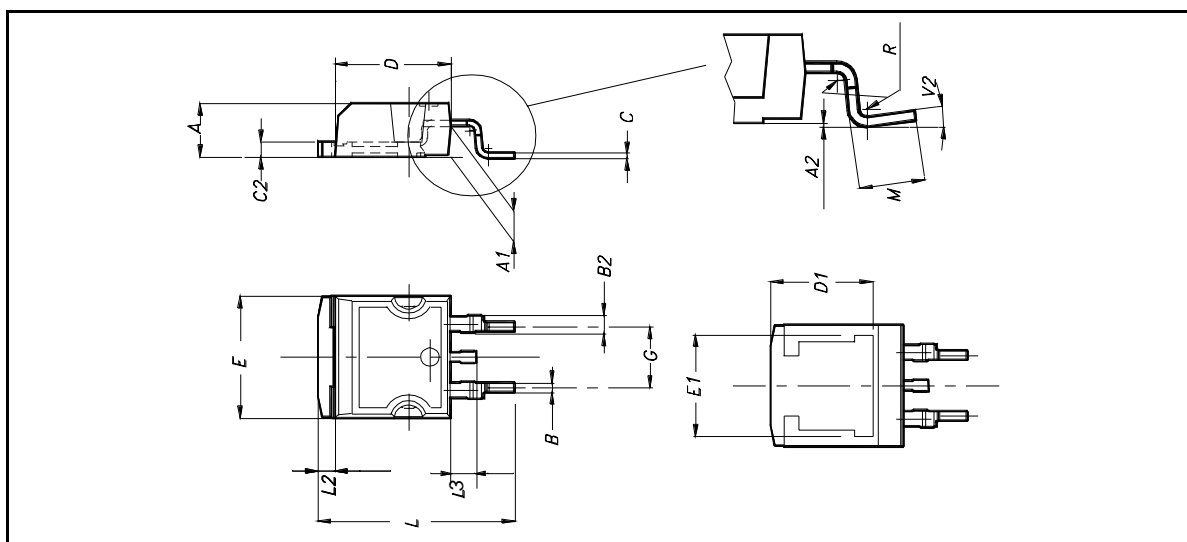
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



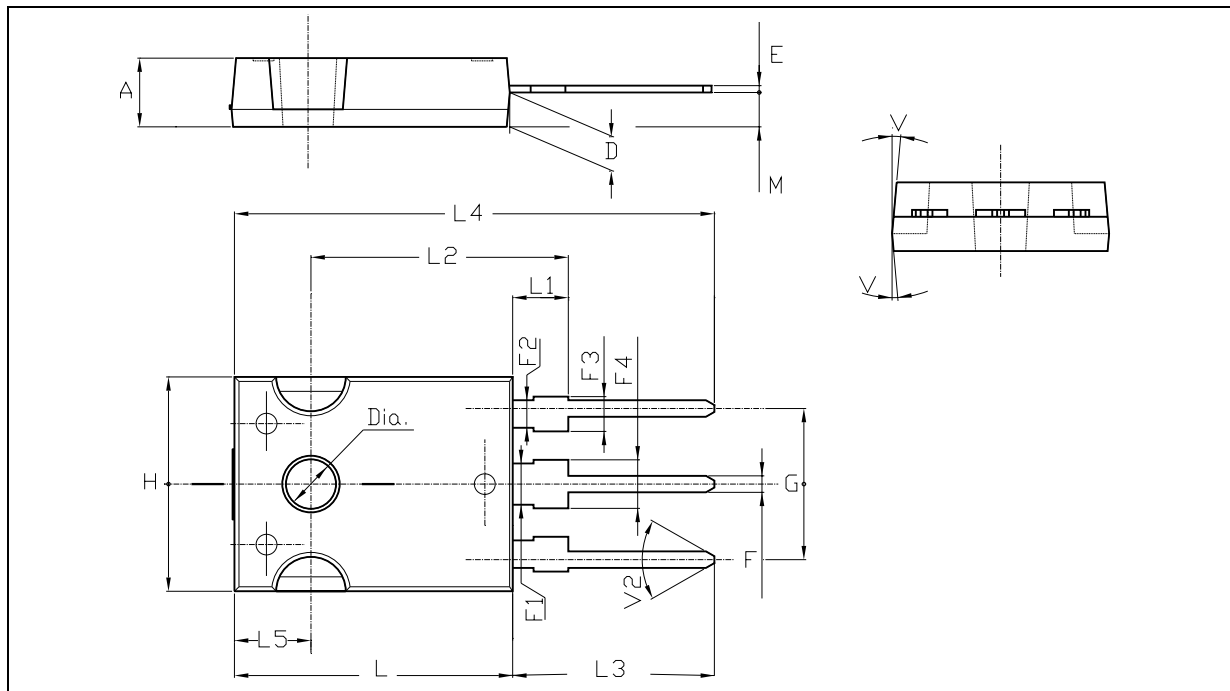
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126



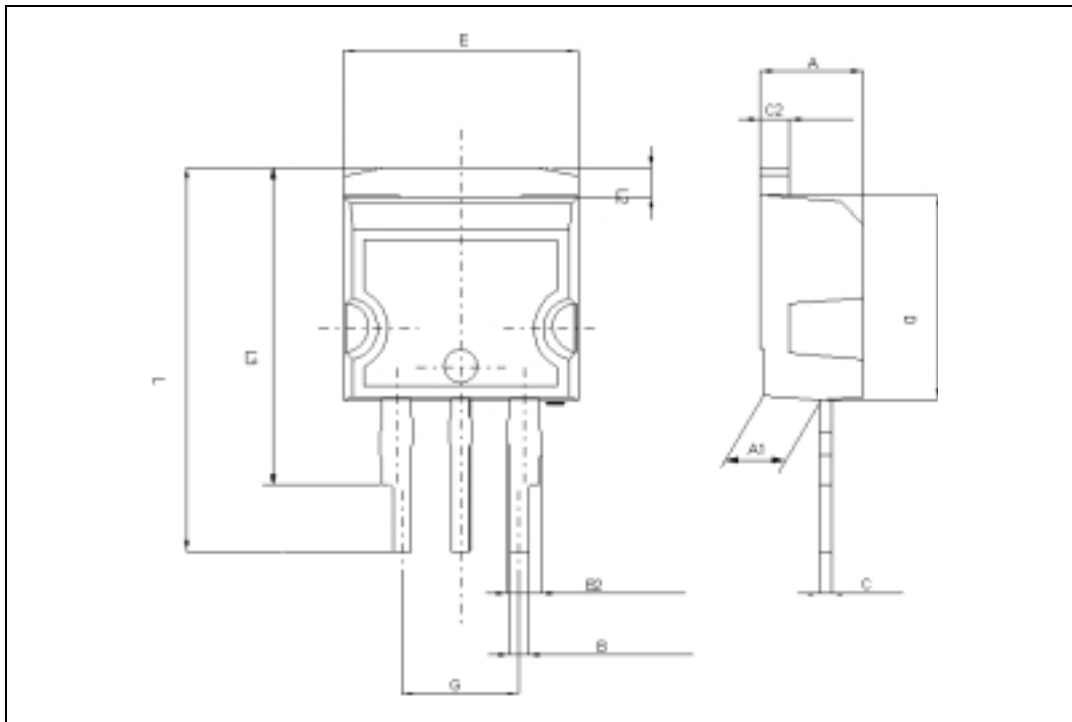
TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
D	2.20		2.60	0.08		0.10
E	0.40		0.80	0.015		0.03
F	1		1.40	0.04		0.05
F1		3			0.11	
F2		2			0.07	
F3	2		2.40	0.07		0.09
F4	3		3.40	0.11		0.13
G		10.90			0.43	
H	15.45		15.75	0.60		0.62
L	19.85		20.15	0.78		0.79
L1	3.70		4.30	0.14		0.17
L2		18.50			0.72	
L3	14.20		14.80	0.56		0.58
L4		34.60			1.36	
L5		5.50			0.21	
M	2		3	0.07		0.11
V		5°			5°	
V2		60°			60°	
Dia	3.55		3.65	0.14		0.143

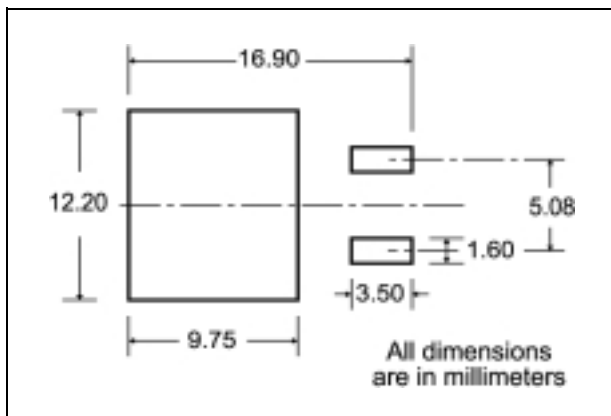


I²SPAK MECHANICAL DATA

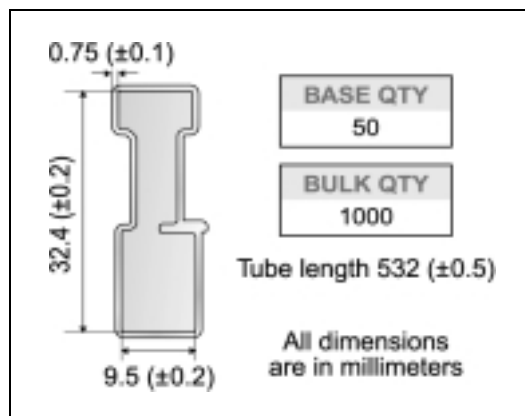
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.70		0.93	0.027		0.037
B2	1.14		1.70	0.045		0.067
C	0.45		0.60	0.018		0.024
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
E	10.00		10.40	0.394		0.409
G	4.88		5.28	0.192		0.208
L	16.7		17.5	0.657		0.689
L2	1.27		1.4	0.05		0.055
L3	13.82		14.42	0.544		0.568



D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*

Diagram showing the tape mechanical data. It includes a circular core with a diameter of 40 mm min. and an access hole at the slot location. The tape slot in the core has a width of 25 mm min. and a full radius. Dimensions A, B, C, D, G, and T are indicated. G is measured at the hub.

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137

Diagrams showing the tape and reel shipment details. The top diagram shows a top view of the tape with dimensions K₀, P₁, P₂, and a 10-pitch cumulative tolerance on tape of +7 - 0.2 mm. The center line of the cavity is indicated. The bottom diagram shows the TRL (Tape Reel Length) and the bending radius R min. The user direction of feed and feed direction are also shown.

* on sales type

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